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Document Identifier: DSP0291

2

Date: 2024-10-29

3

Version: 1.0.0WIP95

4

PCIe Management Interface (PCIe-MI) over MCTP Binding Specification

Information for Work-in-Progress version:

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Supersedes: None

8

Document Class: Normative

9

Document Status: Work in Progress

10

Document Language: en-US

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CONTENTS

| | |
|---|----|
| 1 Foreword | 4 |
| 1.1 Acknowledgments | 4 |
| 2 Introduction | 5 |
| 2.1 Document conventions | 5 |
| 2.1.1 Typographical conventions | 5 |
| 2.1.2 ABNF usage conventions | 5 |
| 3 Scope | 6 |
| 4 Normative references | 7 |
| 5 Terms and definitions | 9 |
| 6 Symbols and abbreviated terms | 10 |
| 7 Conventions | 11 |
| 7.1 Reserved and unassigned values | 11 |
| 7.2 Byte ordering | 11 |
| 8 Overview | 12 |
| 8.1 General | 12 |
| 9 Message type-specific considerations | 13 |
| 9.1 Message type number | 13 |
| 9.2 PCIe-MI over MCTP specification version information | 13 |
| 9.3 Timing specifications | 13 |
| 9.4 PCIe-MI over MCTP message format | 13 |
| 9.4.1 PCIe-MI over MCTP message field descriptions | 14 |
| 9.4.2 Message assembly | 15 |
| 9.5 Maximum message body size | 15 |
| 9.6 Multiple MCTP physical transports | 15 |
| 10 ANNEX A (informative) Change Log | 16 |

16 **1 Foreword**

17 The *PCIe Management Interface (PCIe-MI) over MCTP Binding Specification* (DSP0291) was prepared by the
18 Platform Management Communications Infrastructure (PMCI Working Group) of DMTF.

DMTF is a not-for-profit association of industry members dedicated to promoting enterprise and systems
management and interoperability. For information about DMTF, see <https://www.dmtf.org>.

19 PCI-SIG is a community responsible for developing and maintaining a standardized approach for peripheral
component I/O data transfers. For information about PCI-SIG, see <https://pcisig.com>.

20 **1.1 Acknowledgments**

21 DMTF acknowledges the following individuals for their contributions to this document:

22 **Editor:**

- Austin Bolen — Dell Technologies

23 **2 Introduction**

24 The PCIe Management Interface (PCIe-MI) over MCTP Binding Specification defines an MCTP message type used to transport PCIe-MI payloads to or from PCIe-compatible components over MCTP.

25 **2.1 Document conventions**

26 **2.1.1 Typographical conventions**

27 This document uses the following typographical conventions:

- 28 • Document titles are marked in *italics*.
- 29 • Important terms that are used for the first time are marked in italics.
- 30 • Terms include a link to the term definition in the "Terms and definitions" clause, enabling easy navigation to the term definition.
- 31 • ABNF rules are in monospaced font.

32 **2.1.2 ABNF usage conventions**

33 Format definitions in this document are specified using ABNF (see [RFC5234](#)), with the following deviations:

- Literal strings are to be interpreted as case-sensitive Unicode characters, as opposed to the definition in [RFC5234](#) that interprets literal strings as case-insensitive US-ASCII characters.

34 **3 Scope**

35 The PCIe Management Interface (PCIe-MI) over MCTP Binding Specification defines a binding in order to transport PCIe-MI messages to or from PCIe elements over MCTP. The specific PCIe-MI message contents will be documented outside of DMTF directly by PCI-SIG.

36 Portions of this specification rely on information and definitions from other specifications, which are identified in the [Normative references](#) clause. The following references are particularly relevant:

- DMTF DSP0236, *Management Component Transport Protocol (MCTP) Base Specification 1.3*, defines the MCTP transport protocol over which the PCIe-MI messages are to be transported.

37 4 Normative references

38 The following referenced documents are indispensable for the application of this document. For dated or versioned references, only the edition cited (including any corrigenda or DMTF update versions) applies. For references without a date or version, the latest published edition of the referenced document (including any corrigenda or DMTF update versions) applies. Earlier versions may not provide sufficient support for this specification.

39 DMTF DSP0218, *Platform Level Data Model (PLDM) for Redfish Device Enablement 1.1*, https://www.dmtf.org/sites/default/files/standards/documents/DSP0218_1.1.pdf

40 DMTF DSP0233, *Management Component Transport Protocol (MCTP) I3C Transport Binding Specification 1.0*, https://www.dmtf.org/sites/default/files/standards/documents/DSP0233_1.0.pdf

41 DMTF DSP0235, *NVMe (NVM Express) Management Messages over MCTP Binding Specification 1.0*, https://www.dmtf.org/sites/default/files/standards/documents/DSP0235_1.0.pdf

42 DMTF DSP0236, *Management Component Transport Protocol (MCTP) Base Specification 1.3*, https://www.dmtf.org/sites/default/files/standards/documents/DSP0236_1.3.pdf

43 DMTF DSP0237, *Management Component Transport Protocol (MCTP) SMBus/I2C Transport Binding Specification 1.2*, https://www.dmtf.org/sites/default/files/standards/documents/DSP0237_1.2.pdf

44 DMTF DSP0238, *Management Component Transport Protocol (MCTP) PCIe VDM Transport Binding Specification 1.2*, https://www.dmtf.org/sites/default/files/standards/documents/DSP0238_1.2.pdf

45 DMTF DSP0239, *Management Component Transport Protocol (MCTP) IDs and Codes 1.9*, https://www.dmtf.org/sites/default/files/standards/documents/DSP0239_1.9.pdf

46 DMTF DSP0240, *Platform Level Data Model (PLDM) Base Specification 1.1*, https://www.dmtf.org/sites/default/files/standards/documents/DSP0240_1.1.pdf

47 DMTF DSP0241, *Platform Level Data Model (PLDM) over MCTP Binding Specification 1.0*, https://www.dmtf.org/sites/default/files/standards/documents/DSP0241_1.0.pdf

48 DMTF DSP0248, *Platform Level Data Model (PLDM) for Platform Monitoring and Control Specification 1.2*, https://www.dmtf.org/sites/default/files/standards/documents/DSP0248_1.2.pdf

49 DMTF DSP0261, *NC-SI over MCTP Binding Specification 1.2*, https://www.dmtf.org/sites/default/files/standards/documents/DSP0261_1.2.pdf

50 DMTF DSP0267, *Platform Level Data Model (PLDM) for Firmware Update Specification 1.2*, https://www.dmtf.org/sites/default/files/standards/documents/DSP0267_1.2.pdf

51 DMTF DSP0281, *CXL (Compute Express Link) Type 3 Device Component Command Interface over MCTP Binding Specification 1.0*, https://www.dmtf.org/sites/default/files/standards/documents/DSP0281_1.0.pdf

52 DMTF DSP0283, *MCTP over USB Binding Specification 1.0*, https://www.dmtf.org/sites/default/files/standards/documents/DSP0283_1.0.pdf

- 53 DMTF DSP4014, *DMTF Process for Working Bodies*, <https://www.dmtf.org/sites/default/files/standards/documents/DSP4014.pdf>
- 54 IETF RFC4122, *A Universally Unique Identifier (UUID) URN Namespace*, July 2005, <https://www.ietf.org/rfc/rfc4122.txt>
- 55 IETF RFC5234, *ABNF: Augmented BNF for Syntax Specifications*, January 2008, <https://tools.ietf.org/html/rfc5234>
- 56 ISO/IEC Directives, Part 2, *Rules for the structure and drafting of ISO and IEC documents*, <https://www.iso.org/sites/directives/current/part2/index.xhtml>
- 57 PCI-SIG, *PCI Express® Base Specification*, <https://www.pcisig.com/specifications>

58 **5 Terms and definitions**

59 In this document, some terms have a specific meaning beyond the normal English meaning. Those terms are defined in this clause.

60 The terms "shall" ("required"), "shall not", "should" ("recommended"), "should not" ("not recommended"), "may", "need not" ("not required"), "can" and "cannot" in this document are to be interpreted as described in [ISO/IEC Directives, Part 2](#), Clause 7. The terms in parentheses are alternatives for the preceding term, for use in exceptional cases when the preceding term cannot be used for linguistic reasons. Note that [ISO/IEC Directives, Part 2](#), Clause 7 specifies additional alternatives. Occurrences of such additional alternatives shall be interpreted in their normal English meaning.

61 The terms "clause", "subclause", "paragraph", and "annex" in this document are to be interpreted as described in [ISO/IEC Directives, Part 2](#), Clause 6.

62 The terms "normative" and "informative" in this document are to be interpreted as described in [ISO/IEC Directives, Part 2](#), Clause 3. In this document, clauses, subclauses, or annexes labeled "(informative)" do not contain normative content. Notes and examples are always informative elements.

63 Refer to the MCTP Base Specification ([DSP0236](#)) for terms and definitions that are used across the MCTP specifications.

64 Refer to the [PCI Express Base Specification](#) for terms and definitions applicable to PCIe-MI. For the purposes of this document, the following additional terms and definitions apply.

65 **Endpoint**

66 An MCTP endpoint unless otherwise specified.

67 **PCI Express (PCIe)**

68 An industry-standard low-latency high-bandwidth serial expansion bus for connecting peripheral components to a computer system.

69 **PCIe Management Interface (PCIe-MI)**

70 A management interface defined by PCI-SIG to manage PCIe-compatible components in a PCIe system.

71 **6 Symbols and abbreviated terms**

72 Refer to the MCTP Base Specification ([DSP0236](#)) for symbols and abbreviated terms that are used across the MCTP specifications. Refer to the [PCI Express Base Specification](#) for symbols and abbreviated terms applicable to PCIe-MI. For the purposes of this document, the following additional symbols and abbreviated terms apply.

73 **MCTP**

74 Management Component Transport Protocol

75 **PCIe**

76 PCI Express

77 **PCIe-MI**

78 PCIe Management Interface

79 **7 Conventions**

80 **7.1 Reserved and unassigned values**

81 Unless otherwise specified, any reserved, unspecified, or unassigned values in enumerations or other numeric ranges are reserved for future definition by DMTF.

82 Unless otherwise specified, numeric or bit fields that are designated as reserved shall be written as 0 (zero) and ignored when read.

83 **7.2 Byte ordering**

84 Unless otherwise specified, the byte ordering of multibyte numeric fields or multibyte bit fields in this specification shall be "Big Endian" (i.e., the lowest byte offset holds the most significant byte and higher offsets hold lesser significant bytes).

85 **8 Overview**

86 **8.1 General**

87 PCI Express (PCIe) is an industry standard low-latency, high-bandwidth serial expansion bus for connecting peripheral components to a computer system. The PCIe Management Interface (PCIe-MI) protocol is used for the configuration, control, and status functions in PCIe-compatible components. The PCIe-MI payloads are defined by the [PCI Express Base Specification](#) and the members of PCI-SIG. Refer to <https://pcisig.com> for more information.

88 This specification only defines how PCIe-MI commands are encapsulated in MCTP messages and transferred between MCTP Endpoints over transports that have a corresponding MCTP transport binding specification which is referred to in this document as PCI Management Interface (PCIe-MI) over MCTP. The definitions and semantics of the PCIe-MI payloads themselves are outside the scope of this specification and are defined in the [PCI Express Base Specification](#).

89 The MCTP Transport Bindings that are used for PCIe-MI over MCTP are defined in other companion specifications including but not limited to the MCTP SMBus/I2C Transport Binding Specification ([DSP0237](#)), the MCTP I3C Transport Binding Specification ([DSP0233](#)), the MCTP PCIe VDM Transport Binding Specification ([DSP0238](#)), and the MCTP over USB Binding Specification ([DSP0283](#)).

90 **9 Message type-specific considerations**

91 **9.1 Message type number**

92 The message type number for PCIe-MI messages is defined in the MCTP IDs and Codes Specification ([DSP0239](#)) and the number assigned is 0x09.

93 **9.2 PCIe-MI over MCTP specification version information**

94 Implementations that follow this specification shall return the following version information in the response to the GET MCTP Version Support command when the Message Type parameter in the request is set to 0x09 (return PCI Management Interface (PCIe-MI) over MCTP Specification version information).

95 The Version Number Entry 1 field shall be used to indicate compatibility with Version 1.0 of the PCIe-MI over MCTP message type as:

96 1.0 [Major version 1, minor version 0, any update version, no alpha]

97 This is reported using the encoding as: 0xF1F0FF00

98 **9.3 Timing specifications**

99 PCIe-MI over MCTP messages are made up of one or more MCTP packets. Each MCTP packet shall comply with the timing, arbitration, and fairness requirements of the transport binding specifications for the media through which it passes. For examples, refer to the specific MCTP physical layer binding specification (for example the MCTP SMBus/I2C Transport Binding Specification ([DSP0237](#)), the MCTP I3C Transport Binding Specification ([DSP0233](#)), the MCTP PCIe VDM Transport Binding Specification ([DSP0238](#)), and the MCTP over USB Binding Specification ([DSP0283](#)), among others) for specific packet and message timing requirements.

100 **9.4 PCIe-MI over MCTP message format**

101 Referring to [Figure 1](#), the PCIe-MI over MCTP messages are carried via the MCTP packet payload of one or more MCTP packets.

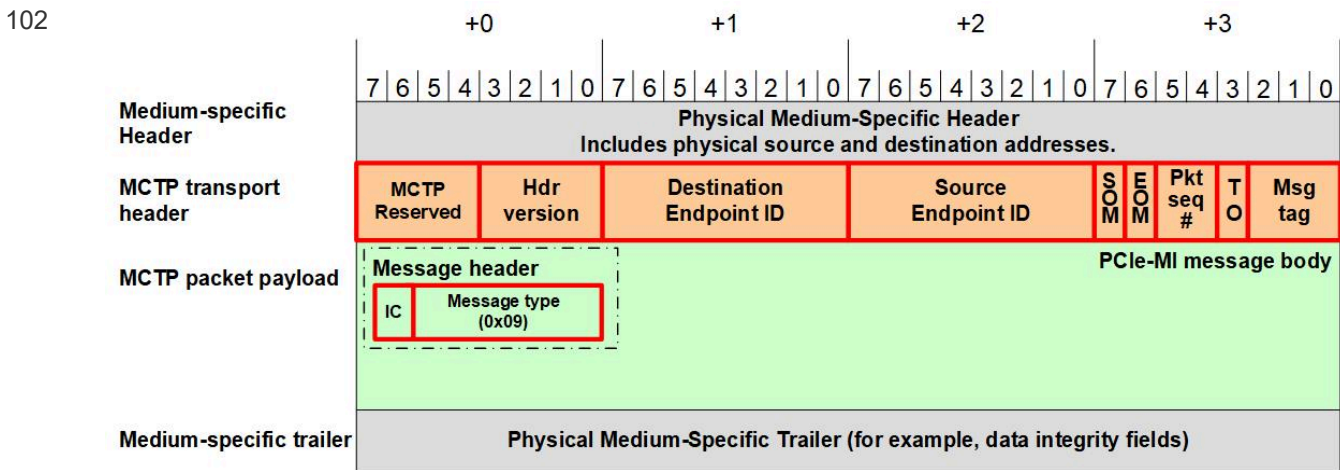


Figure 1 — PCIe-MI over MCTP Message Fields in an MCTP Packet

9.4.1 PCIe-MI over MCTP message field descriptions

PCIe-MI message fields shall comply with the requirements in the MCTP Base Specification (DSP0236) and with the additional requirements indicated in Table 1.

Table 1 — PCIe-MI over MCTP Message Field Descriptions

| Field Name | Field Size | Description |
|-----------------------|------------|--|
| Tag Owner (TO) | 1 bit | 1b - PCIe-MI Request messages. 0b - PCIe-MI Response messages. A PCIe-MI Response message shall use the destination EID and physical address that were used as the source EID and source physical address of the corresponding PCIe-MI Request message. |
| Message Tag (Msg tag) | 3 bits | When request/response message exchange is used and the Tag Owner (TO) bit is set to 1b in the PCIe-MI Request message, a responder shall return the same Message Tag with the Tag Owner bit cleared to 0b in the corresponding PCIe-MI Response message. |
| Integrity Check (IC) | 1 bit | Message Integrity Check bit = 0b. PCIe-MI over MCTP messages do not include an overall Message Integrity check field. |
| Message type | 7 bits | The PCIe-MI over MCTP message type number shall be set to 0x09. This field identifies the MCTP message as carrying a PCIe-MI over MCTP message. |
| PCIe-MI message body | Variable | Other than the message type field and the IC bit, the PCIe-MI message body is defined by PCIe-MI. |

For the definition of PCIe-MI Request Message, PCIe-MI Response Message, and the PCIe-MI message body other than the message type field and the IC bit, refer to the [PCI Express Base Specification](#).

108 **9.4.2 Message assembly**

109 PCIe-MI over MCTP messages may be split into one or more MCTP packets thus requiring segmentation and assembly. All multi-packet PCIe-MI over MCTP messages shall comply with the message packetization and assembly rules of the MCTP Base Specification ([DSP0236](#)). Specifically, sections in the MCTP Base Specification ([DSP0236](#)) related to Message assembly, Dropped packets, Starting message assembly, Terminating message assembly/dropped messages, and Dropped messages shall be complied with. PCIe-MI messages when transported over MCTP shall not require any changes to the MCTP Base Specification ([DSP0236](#)).

110 **9.5 Maximum message body size**

111 The PCIe-MI over MCTP message body shall be less than or equal to 4224 (4K+128) bytes. All MCTP endpoints that support PCIe-MI shall support this maximum message body size of 4224 bytes. This corresponds to a transfer of 66 MCTP packets using a baseline transmission unit of 64 bytes for the MCTP packet payload. See the [PCI Express Base Specification](#) for a definition of the PCIe-MI message payload and headers.

112 The maximum message body size includes the IC bit, the message integrity check field, the message type field, and any additional message type-specific header fields required by PCIe-MI. Refer to the [PCI Express Base Specification](#) for any additional restrictions on message body sizes.

113 **9.6 Multiple MCTP physical transports**

114 In order to facilitate identification of PCIe-compatible components that are accessible via multiple physical transports, endpoints that support PCIe-MI shall support the Get Endpoint UUID MCTP command.

115 Otherwise, this specification does not define any additional behaviors related to communicating with endpoints that support PCIe-MI over MCTP that may be accessed through more than one type of MCTP physical transport on a given MCTP network.

116

10 ANNEX A (informative) Change Log

| Version | Date | Description |
|------------|------------|--------------------------|
| 1.0.0WIP95 | 2024-10-29 | Work-in-progress release |