

# Update on Redfish Support for Compute Express Link (CXL)





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### Agenda

Status of CXL in Redfish The Chassis and System Model for CXL

- PCIe Devices/Functions
- CXL Logical Devices
- Memory Domains and Memory Chunks for CXL Memory

#### Modeling Local CXL Devices

- Type 1 Devices (SmartNICs)
- Type 2 Devices (Accelerators)
- Type 3 Devices (Memory Buffers)

- Modeling Remote CXL Devices
  - Type 1 Devices

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- Type 2 Devices
- Type 3 Devices
- DCD Models
- Example Redfish Resources

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# **Status of CXL in Redfish**

#### Current State of Fabrics Model

- Fabric model supporting CXL 2.0 are complete
- Some CXL 3.0 models have been added
  - Basic DCD
  - CXL Switch Basic Configuration
  - Recommend start with Redfish version 2025.1
- DSP\_0288 Redfish Mapping Spec v1.2 has been released
  - Needs some review from implementers
  - Currently being updated with recent changes

#### What we are working on (Fabric Task Force Work Items)

- Dynamic Capacity Devices
- Rosetta Stone on new capabilities in v3.1 of CXL Specification
- Current redfish model requires a high-level orchestrator
  - Currently, no redfish construct that takes CXL CCI information for global memory and have it persist if you get rid of memory region. (No Logical Memory Region).
  - We have a WIP published for Logical Memory Regions and would like your feedback
  - DSP-IS0020\_1.0.0WIP50.zip

# **CXL Device Base Redfish Model**





- CXL management model built on top of Redfish PCIe model
- CXL Device can provide standard PCIe Functions as well as extended functions supporting new CXL cache and memory semantics
- New CXL Logical Device allows partitioning of device resources and binding to different hosts through CXL switch
- PCIe Functions may be flexibly associated with CXL Logical Devices thus bound to different compute host (future functionality not defined in current specification)
- All PCIe Functions supporting CXL extensions associated with CXL Logical Device can use resources (e.g., memory) referenced by these devices



# **CHASSIS AND SYSTEM MODEL FOR CXL**



# Chassis Model for CXL Device

- CXL devices are not always bound to a specific host physically
- CXL device objects are located in the Chassis Model
  - · Chassis describes resources within the chassis
  - Remote accelerators on a CXL fabric can also reside in Chassis
- PCIeDevice in Chassis describes CXL devices in the chassis
  - Fabric Manager can create Memory Chunks to be available for assignment
  - Assignment is done through the CXL Logical
     Device
- Devices in Chassis describes a remote resource
  - Shown here is a processor however other devices such as memory or I/O could also be represented here



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# **System Model for CXL**

- System describes a host that is attached to a CXL fabric
  - Ports of processor describes how the system is connected to the fabric
  - 'Memory' can contain remote memory that describes memory bound to the host over the fabric
- MemoryDomain in system can describe either locally attached CXL memory or remote CXL memory
- MemoryChunk in system describes a section of address space backed by local or remote memory
  - Can be interleaved or a contiguous range across local or remote devices
- Memory describes a logical memory device that represents the memory that is assigned to this host over the CXL Fabric





Attached directly to Computer System

# LOCAL CXL DEVICE MODELS















Attached to Computer System through Fabric

# **REMOTE CXL DEVICE MODELS**

















Switch attached

# **DYNAMIC CAPACITY DEVICES**



The maximum dynamic

capacity for each region

is divided into per region

fixed sized blocks

A single extent list is maintained for each

host by the DCD & reports the blocks

currently added to the host for all region

## **CXL Dynamic Capacity Device**

Dynamic Capacity is a feature of a CXL memory device that allows memory capacity to change dynamically without the need for resetting the device DCD controls the allocation of these DC blocks to the host which requires appropriated management APIs to be defined

DP/



The devices' maximum

dynamic capacity for all

regions programmed into

one or more HDM decoders



# **Redfish CXL Model Changes**

### New resource to model memory region

- Memory regions are defined per host so they should be subordinates of the CXL Logical Device
- Physical memory is provided to memory region by multiple memory chunks
- Memory region capacity is exposed to the host using extent list

#### Resources updated

- PCle Device
- CXL Logical Device
- Memory
- Memory Chunks
- Connection



Source: CXL 3.0 Specification











# **EXAMPLE RESOURCES**



# **CXL Logical Device**

Remote CXL Logical Device





# **Remote Memory at Host**

Showing memory in the host from a Remote source





## **Memory Chunk**

Memory range accessible by Host

{	/1/MemoryChunks/1". Men	nory chunk is in remote chassis PCXI 3
"Id": "1",		
"Name": "Memory Chunk 1",		
"Description": "Memory chunk accessible through CXL f	abric",	
"MemoryChunkSizeMiB": 4096,	Tot	al Size of this Memory Chunk
"AddressRangeType": "PMEM",	Mar	
"AddressRangeOffsetMiB": 1024,	Mer	nory Type and offset within this CXL Device
"MediaLocation": "Local",		
"RequestedOperationalState": "Online",		
"Links": {		
"CXLLogicalDevices": [		Logical Device that is exporting this
{ "@odata.id": "/redfish/v1/Chassis/PCXL3/PCI	eDevices/1/CXLLogicalDevices/1"	Memory Chunk
"Endpoints": [		
{ "@odata.id": "/redfish/v1/Fabrics/CXL/Endpo	ints/T3" }	Endpoint of this device on the CXL Fabric
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# **DCD EXAMPLES**

## **Memory Region Schema**

- New schema defining Memory Region with following properties
  - Region Number
  - Region Type
    - Static static memory region
    - Dynamic dynamic memory region supporting dynamic capacity
  - Region Base offset (DPA addressable)
  - Region Size
  - Flag indicating shareable region
  - Flag indicating memory needs to be sanitized during deallocation
  - Flag indicating Non-Volatile memory region
  - Flag indicating support for hardware managed coherency
  - Region memory block size
  - Extents Count (Dynamic Memory Region only)
  - Array of Memory Extents (Dynamic Memory Region only)
    - Memory Extent Offset (DPA addressable)
    - Memory Extent Size
    - Extent user-defined Tag
    - Host Extent Sequence Number
    - Array of memory chunks providing capacity for memory region
      - Chunk Offset within memory region
      - Link to memory chunk

```
"Id": "1",
"Name": "CXL Memory Region",
 "Description": "CXL Memory Region",
 "Status": {
    "State": "Enabled".
    "Health": "OK",
    "HealthRollup": "OK"
 "RegionType": "Static | Dynamic",
"RegionNumber": 0.
"RegionBaseOffetMiB" 8192
"RegionSizeMiB": 65536.
 "NonVolatileRegion": false,
"HardwareManagedCoherencyRegion": true,
 "SanitizeOnRelease": false.
 "BlockSizeMiB": 128.
         "ExtentOffsetMiB": 1024,
        "ExtentSizeMiB": 4096.
         "Tag": "User Defined Tag"
         "SequenceNumber": 0
1,
        "ChunkOffsetMiB": 1024.
        "ChunkLink": {
            "@odata.id": "/redfish/v1/Chassis/CXL/MemoryDomain/1/MemoryChunks/1"
],
"Oem": {},
"@odata.id": "/redfish/v1/Chassis/CXL/PCIeDevices/1/CXLLogicalDevices/1/MemoryRegions/1"
```

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## **PCle Device Schema**

- Existing schema updated with new property

   Dynamic Capacity containing DCD attributes
  - Number of hosts supported by the dynamic capacity device
  - Number of memory regions supported by the device dynamic capacity
  - Total dynamic memory capacity of the device
  - List of supported Add Capacity Policies
  - List of supported Remove Capacity Policies
  - List of supported Memory Block Sizes per Memory Region
  - Flag indicating support for memory
     sanitization on release per Memory Region

```
"Id": "1".
"Name": "CXL DCD",
"Description": "CXL Device supporting dynamic capacity",
"CXLDevice": {
    "DynamicCapacity":{
        "MaxHosts": 1.
        "MaxDynamicCapacityRegionsNumber": 1,
        "TotalDynamicCapacityMiB": 65536,
        "AddCapacityPoliciesSupported":
            "Free", "Contiguous", "Prescriptive"
        "ReleaseCapacityPoliciesSupported":
            "Tag-based", "Prescriptive"
        "MemoryBlockSizesSupported":[
                "RegionNumber": 0,
                "BlockSizeMiB": [ 64, 128, 256, 512, 1024 ]
        "SanitizationOnReleaseSupported":[
                "RegionNumber": 0,
                "SanitizationConfigurable": true
'@odata.id": "/redfish/v1/Chassis/CXL/PCIeDevices/1"
```



## **CXL Logical Device Schema**

- Existing schema updated with new properties
  - Link to collection of Memory Regions defined for CXL
     Logical Device

```
{
    "Id": "1",
    "Name": "CXL Logical Device",
    "Description": "CXL Logical Device supporting dynamic memory capacity",
    "MemoryRegions": {
        "@odata.id": "/redfish/v1/Chassis/CXL/PCIeDevices/1/CXLLogicalDevices/1/MemoryRegions"
    },
    "@odata.id": "/redfish/v1/Chassis/CXL/PCIeDevices/1/CXLLogicalDevices/1"
```



### **Memory Schema**

- Existing schema updated with new properties
  - Array of links to Memory Regions providing media for
     logical memory device

"Td", "1"
IV. I, "System CM logical memory device"
"Description". "System logical memory davice representing remote CVI Memory Region"
"Links": {
"MemoryRegionMediaSources": [
{
"@odata.id": "/redfish/v1/Chassis/CXL/PCIeDevices/1/CXLLogicalDevices/1/MemoryRegions/1"
}
]
},
"@odata.id": "/redfish/v1/Systems/1/Memory/1"



## **Memory Chunks Schema**

- Existing schema updated with new properties
  - Array of links to Memory Regions exposing memory provided by this Memory Chunk

```
{
    "Id": "1",
    "Name": "Memory Chunk 1",
    "Description": "Physical Memory Chunk providing capcity for CXL Memory Regions",
    "Links": {
        "MemoryRegions": [
            { "@odata.id": "/redfish/v1/Chassis/CXL/PCIeDevices/1/CXLLogicalDevices/1/MemoryRegions/1" }
    ]
    },
    "@odata.id": "/redfish/v1/Chassis/CXL/MemoryDomains/1/MemoryChunks/1"
```



# **Connection Schema**

- Existing schema updated with new properties
  - Memory Region Info defining connection properties for memory region



## **Additional Resources**

- More details of the CXL model can be found at the CXL Public Mockup on the DMTF Website <u>https://redfish.dmtf.org</u>
- The Fabrics Whitepaper provides details of the redfish fabrics model and example fabric types
  - <u>https://www.dmtf.org/sites/default/files/standards/documents/DSP2066</u>
     <u>1.0.0.pdf</u>



### Thank you!

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